Chou et al. Nanoscale Res Lett (2021) 16:125
https://doi.org/10.1186/s11671-021-03577-0

Nanoscale Research Letters

NANO EXPRESS

Ge N-Channel MOSFETs with ZrO_2 Dielectric Achieving Improved Mobility

Lulu Chou[1], Yan Liu[1], Yang Xu[1], Yue Peng[1], Huan Liu[1,2], Xiao Yu[2*], Genquan Han[1*] and Yue Hao[1]

Abstract

High-mobility Ge nMOSFETs with ZrO_2 gate dielectric are demonstrated and compared against transistors with different interfacial properties of ozone (O_3) treatment, O_3 post-treatment and without O_3 treatment. It is found that with O_3 treatment, the Ge nMOSFETs with ZrO_2 dielectric having a EOT of 0.83 nm obtain a peak effective electron mobility (μ_{eff}) of 682 cm^2/Vs, which is higher than that of the Si universal mobility at the medium inversion charge density (Q_{inv}). On the other hand, the O_3 post-treatment with Al_2O_3 interfacial layer can provide dramatically enhanced-μ_{eff}, achieving about 50% μ_{eff} improvement as compared to the Si universal mobility at medium Q_{inv} of 5×10^{12} cm^{-2}. These results indicate the potential utilization of ZrO_2 dielectric in high-performance Ge nMOSFETs.

Keywords: Germanium, ZrO_2, MOSFET, CMOS, Mobility

Background

GERMANIUM (Ge) has exhibited advantages of higher carrier mobility and lower processing temperature compared with Si devices. These make Ge to be an alternative for applications of ultrascaled CMOS logic devices and thin-film transistors (TFTs) as top layer in three-dimensional integrated circuits [1–3]. In the past few years, great efforts have been focused on surface passivation, gate dielectric, and channel engineering for Ge p-channel metal–oxide–semiconductor field-effect transistors (MOSFETs), which have contributed to significant improvement in electrical performance for the p-channel devices.

But for Ge n-channel MOSFETs, low effective carrier mobility (μ_{eff}) caused by poor interfacial layer of gate stack strongly limits the performance of the devices. Various surface passivation techniques including Si passivation [1], plasma post-oxidation [4], and InAlP passivation [5] and several high-κ dielectrics including HfO_2, ZrO_2 [6–8], Y_2O_3 [9], and La_2O_3 [10] have been explored in Ge nMOSFETs to boost the electron μ_{eff}. It was demonstrated that ZrO_2 dielectric integrated with Ge channel can provide a robust interface due to that a GeO_2 interfacial layer can react and intermix with the ZrO_2 layer [7]. A decent hole μ_{eff} has been reported in Ge p-channel transistors [6–8], while there is still a lot of room for improvement in electron μ_{eff} for their counterparts.

In this work, Ge nMOSFETs with ZrO_2 gate dielectric are fabricated to achieve improved μ_{eff} over Si in the entire range of inversion charge density (Q_{inv}). Ge transistors obtain a 50% improvement in electron μ_{eff} compared to the Si universal mobility at a medium Q_{inv} of 5.0×10^{12} cm^{-2}.

Experimental

The key process steps for fabricating Ge nMOSFETs on 4-inch p-Ge(001) wafers with a resistivity of 0.136–0.182 Ω cm are shown in Fig. 1a. The source/drain (S/D) regions were implanted with phosphorous ion at a dose of 1×10^{15} cm^{-2} and an energy of 30 keV followed by dopant activation annealing at 600 °C. After the pre-gate cleaning, Ge wafers were loaded into an atomic layer deposition chamber for the formation of the gate dielectric layer(s): Al_2O_3/O_3 oxidation/ZrO_2, ZrO_2, or O_3

*Correspondence: yuxiao@zhejianglab.com; gqhan@xidian.edu.cn
[1] State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, People's Republic of China
[2] Intelligent Chip Research Center, Zhejiang Lab, Hangzhou 311121, People's Republic of China

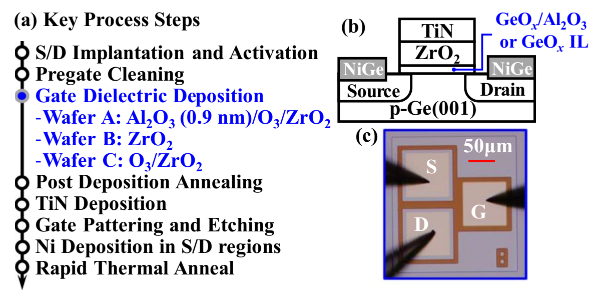

Fig. 1 **a** Key process steps for fabricating Ge nMOSFETs. **b** Cross-sectional schematic and **c** microscope image of the fabricated devices

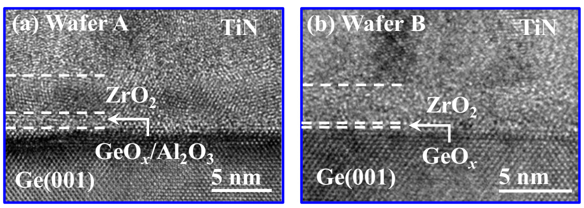

Fig. 2 HRTEM images of **a** TiN//ZrO_2/Al_2O_3/GeO_x/Ge, **b** TiN/ ZrO_2/GeO_x/Ge stacks for the devices on wafers A and B, respectively

oxidation/ZrO_2 for wafers A, B, or C, respectively. For wafer A, 0.9 nm Al_2O_3 was used to protect the channel surface during O_3 oxidation. O_3 oxidation was carried out at 300 °C for 15 min for both wafers A and C. For all the wafers, the thickness of ZrO_2 was ~3.3 nm. Subsequently, TiN(100 nm) gate metal was deposited via physical reactive sputtering, and lithography patterning and reactive ion etching were used to form the gate electrode. After that, a 25-nm-thick Ni layer was deposited in S/D regions. Finally, the post-metallization annealing (PMA) at 350 °C for 30 s was carried out to form the Ni germanide and improve the interface quality. Schematic and microscope images of the fabricated transistor are shown in Fig. 1b, c, respectively.

Figure 2a, b shows the high-resolution transmission electron microscope (HRTEM) images of the gate stacks on wafers A and B, respectively. The unified thickness of the Al_2O_3/GeO_x interfacial layer (IL) for wafer A is ~1.2 nm indicating the 0.2–0.3 nm GeO_x. For the device on wafer B, an ultrathin GeO_x IL was experimentally demonstrated [7].

Results and Discussion

The measured capacitance (*C*) and the leakage current (*J*) characteristics for Ge MOS capacitors on wafers A, B, and C are measured and shown in Fig. 3a, b, respectively. The equivalent oxide thickness (EOT) of the devices on wafers A, B, and C is extracted to be 1.79, 0.59, and 0.83 nm, respectively. Assuming the GeO_x IL provides an extra EOT of ~0.25 nm for wafers A and C by comparing wafers B and C, the 3.3 nm ZrO_2 contributes an EOT of ~0.6 nm with κ value of ~21.8, which is consistent with the previous reported value of amorphous ZrO_2 [11]. These derived results also confirm that the thickness in GeO_x IL on wafer B is negligible.

The GeO_x/Al_2O_3 IL for wafer A and GeO_x IL for wafer C produces the EOT of ~1.2 and ~0.25 nm, respectively. The EOT of the devices can be further reduced by decreasing the IL thickness or improving the interface quality, and enhancing the permittivity of ZrO_2 with some surface passivation, e.g., NH_3/H_2 plasma treatment [6]. Figure 3c compares *J* versus EOT characteristics for the Ge nMOSFETs in this work against values for other reported Ge devices [5, 12–17]. It is also observed that the results are consistent with the reported Ge MOS with ultra-thin EOT following the same trends, indicating the difference of leakage current shown in Fig. 3b should be mainly attributable to the difference of EOT.

Figure 4a shows measured drain current (I_D) and source current (I_S) versus gate voltage (V_G) curves of Ge nMOSFETs from wafers A, B, and C. All transistors have a gate length L_G of 4 μm and a gate width W of 100 μm. The point subthreshold swing (SS), defined as $dV_G/d(\log I_D)$, as a function of I_D curves for the transistors in Fig. 4a is calculated and shown in Fig. 4b. It is clarified that the transistor on wafer A exhibits the degraded I_D leakage floor and SS compared to the devices on wafers B and C. Besides the increase in EOT in devices on wafer A would bring in the increment of SS, these phenomenon should be partly attributed to the fact that the device with the Al_2O_3 inserted layer has a higher density of interface traps (D_{it}) within the bandgap of the Ge channel in comparison with the wafers B and C.

Figure 4c shows the measured output characteristics, i.e., I_D–V_D curves for various values of gate overdrive $|V_G-V_{TH}|$ of the devices demonstrating that the Ge transistor on wafer A achieves significantly improved drive current compared to the devices on wafers B and C. Here, V_{TH} is defined as V_{GS} corresponding to an I_D of 10^{-7} A/μm. Considering the identical conditions for S/D formation, the boosted I_{DS} for transistors on wafer A indicates the higher μ_{eff} [18–21]. The Al_2O_3 layer has not led to the degradation of D_{it} performance near the conduction band of the Ge channel.

Figure 5a shows the total resistance R_{tot} as a function of L_G for the Ge nMOSFETs with ZrO_2 dielectric with an L_G ranging from 2 to 10 μm. The values of R_{tot} are extracted at a gate overdrive of 0. 6 V and a V_D of 0.05 V. The S/D resistance R_{SD} of the transistors is extracted to be ~13.5 kΩ μm, utilizing the fitted lines intersecting at

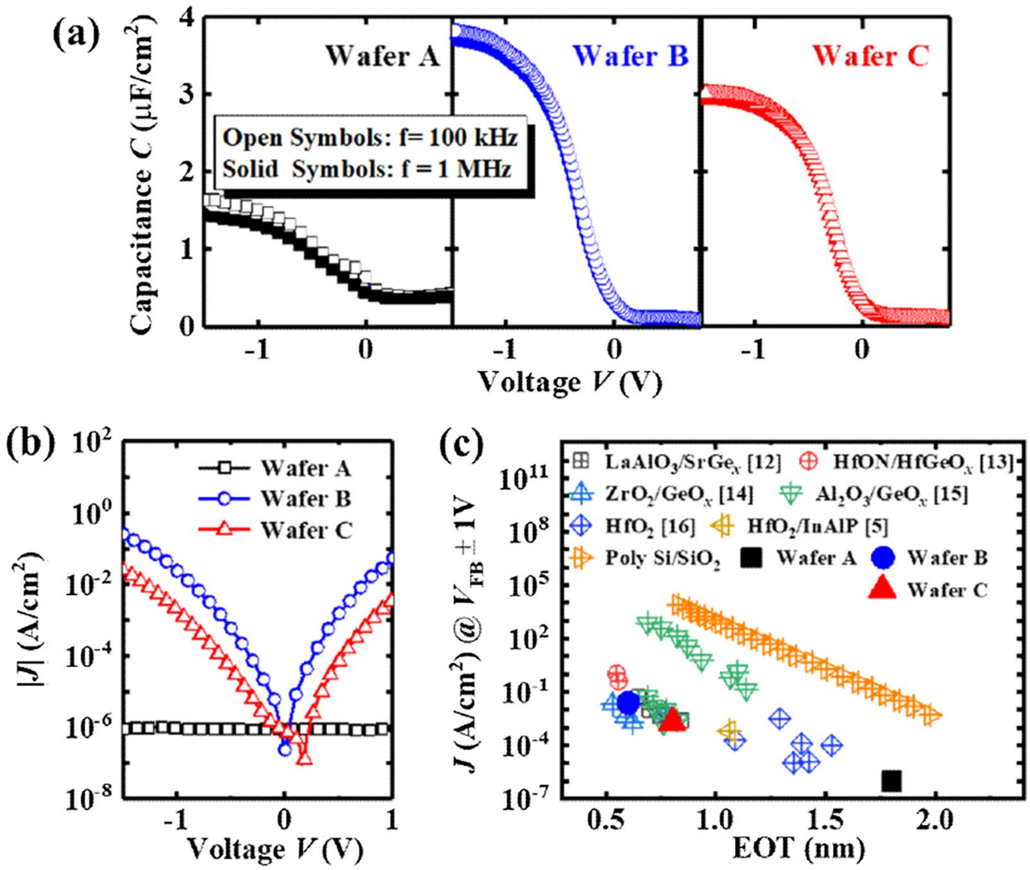

Fig. 3 **a** Measured *C* as a function of voltage *V* characteristics for Ge pMOS capacitors on wafers A, B, and C. **b** *J* versus *V* curves for the devices. **c** Benchmarking of *J* (extracted at $V_{FB} \pm 1$ V) of the Ge MOS capacitors in this work against data obtained for similar bias conditions from the literature

the *y*-axis. The similar R_{SD} is consistent with the identical process of PMA and S/D formation. The channel resistance R_{CH} values of the devices are obtained by the slope of the fitted lines, i.e., $\Delta R_{tot}/\Delta L_G$, which can be used for calculating the μ_{eff} characteristics of Ge nMOSFETs. To evaluate the interface quality, interface trap densities (D_{it}) were extracted by the following equation according to Hill's method [17]:

$$D_{it} = \frac{2G_{m\,max}/\omega}{qA\left[\left(\frac{G_{mmax}}{\omega C_{ox}}\right) + (1 - C_m/C_{ox})^2\right]}$$

where q is the electronic charge, A is the area of the capacitor, $G_{m,max}$ is the maximum value of measured conductance, with its corresponding capacitance C_m, ω is the angular frequency, and C_{ox} is gate oxide capacitance. The D_{it} values are calculated to be 3.7, 3.2, and 2.3×10^{12} eV^{-1} cm^{-2} for the devices on wafers A, B, and C, respectively.

It is known that the calculated values correspond to the midgap D_{it}. The device with Al_2O_3 IL on wafer A has a higher midgap D_{it} compared to the devices on wafers B and C. This is consistent with the results in Figs. 3a and 4a, and the higher midgap D_{it} gives rise to a larger depletion capacitance dispersion in wafer A causing a higher leakage current of I_{DS} in comparison with the other two wafers. Note the wafer A should have the lower D_{it} near the conduction bandgap due to its higher μ_{eff} over wafers B and C.

It is well known that μ_{eff} is the bottleneck for high drive current and transconductance in Ge nMOSFETs. Here, μ_{eff} can be calculated by $\mu_{eff} = 1/[WQ_{inv}(\Delta R_{tot}/\Delta L_G)]$, where $\Delta R_{tot}/\Delta L_G$ is the slope of the R_{tot} versus L_G as shown in Fig. 5a. Q_{inv} can be obtained by integrating the measured C_{inv}–V_G curves. In Fig. 5b, we compare the μ_{eff} versus Q_{inv} of the Ge nMOSFETs on wafers A, B, and C with those reported previously in [18, 22–25]. The extracted peak μ_{eff} values of the transistors on wafers A and C are 795 and 682 cm^2/V s, respectively, and that of Ge nMOSFETs on wafer B is 433 cm^2/V s. Ge nMOSFETs with Al_2O_3 IL achieve a significantly improved μ_{eff} in comparison with the transistors on wafer B or C, the devices

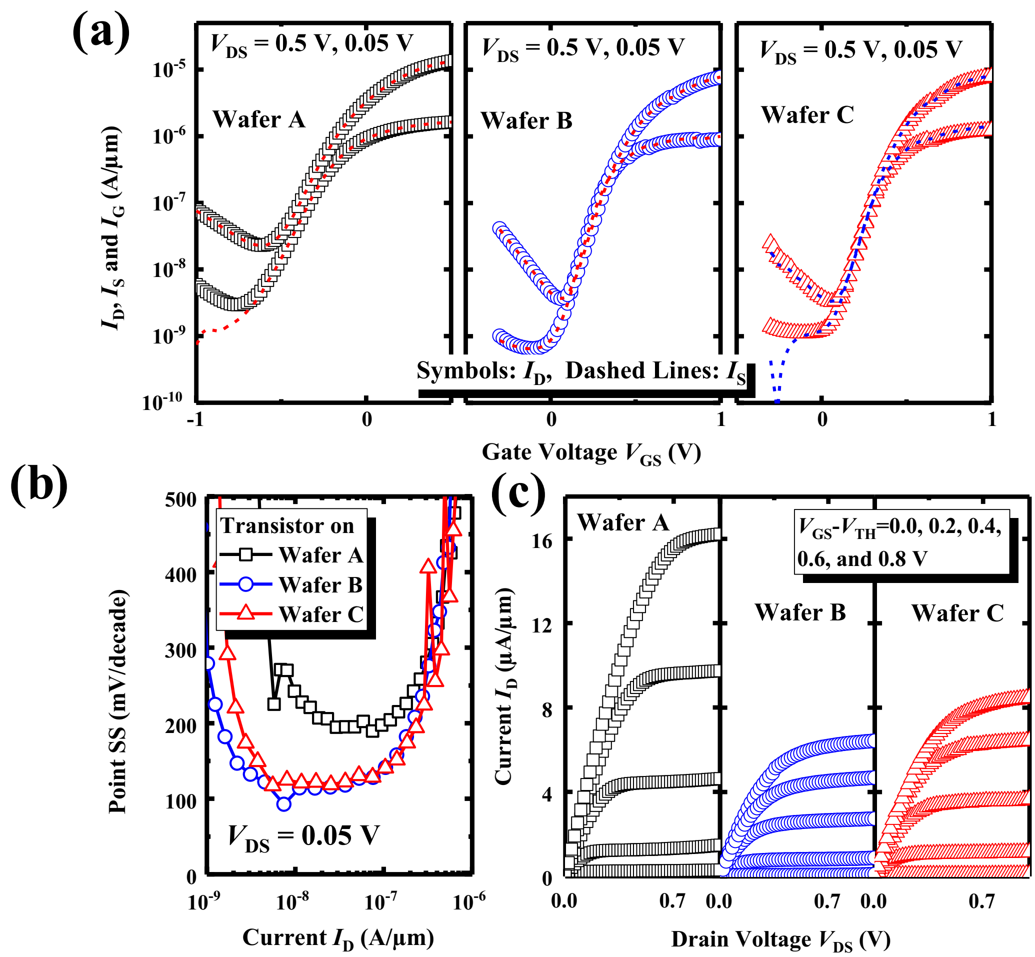

Fig. 4 **a** Measured I_D and I_S versus V_{GS} curves of Ge nMOSFETs on wafers A, B, and C. **b** Point SS as a function of I_D for the transistors. **c** I_D–V_D characteristics show that the Ge nMOSFET on wafer A has a higher drive current compared to the devices on wafers B and C

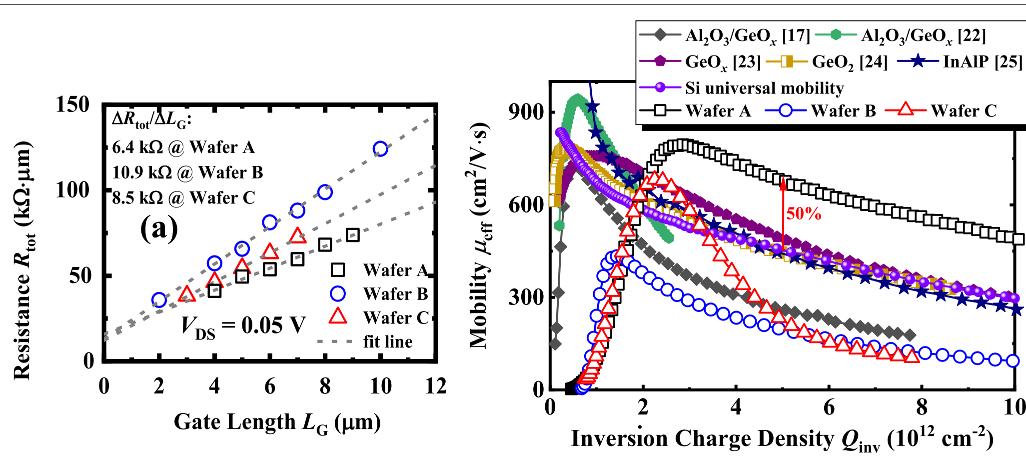

Fig. 5 **a** R_{tot} versus L_G curves for Ge nMOSFETs on wafers A, B, and C. The fitted line intersecting at the y-axis and the slope of linear fit lines are utilized to extract the R_{SD} and R_{CH}, respectively. **b** μ_{eff} for the Ge nMOSFETs in this work versus previously published results for unstrained Ge transistors. The devices on wafer A show the improved μ_{eff} than the Si universal mobility in the entire range of Q_{inv}

in [18, 22–25] in a high field, and Si universal mobility in the entire Q_{inv} range. At a Q_{inv} of 5×10^{12} cm^{-2}, a 50% μ_{eff} enhancement is achieved in devices on wafer A as compared to the Si universal mobility. This demonstrates that by protecting the channel surface for preventing the intermixing of ZrO_2 and GeO_x using Al_2O_3, a high-quality interface between gate insulator and Ge is realized to boost the mobility characteristics, which is also reported in the previous studies of Ge MOSFETs with ultrathin EOT [26]. μ_{eff} in transistors on wafer C is higher than the Si universal at a Q_{inv} of 2.5×10^{12} cm^{-2}, although it rapidly decays with the increase in Q_{inv} range. This indicates that the used O_3 oxidation before ZrO_2 deposition would improve the interfacial quality to some extent; however, it does not lead to enough flat channel surface to effectively suppress the surface roughness scattering of the carrier at high Q_{inv} due to the intermixing of ZrO_2 and GeO_x, since it is reported that the generation of oxygen vacancies during the intermixing would increase the short-range order (SRO) roughness [27]. Optimizing the O_3 oxidation process or reducing the Al_2O_3 IL thickness can make the Ge transistor achieve a reduced EOT while maintaining a higher μ_{eff} at the high Q_{inv}.

Conclusions

The impacts of gate dielectric structure and morphology on Ge nMOSFET electrical characteristics are investigated. An Al_2O_3/ZrO_2 gate dielectric provides for significantly-improved μ_{eff} as compared to the Si universal mobility. μ_{eff} can be improved by inserting an Al_2O_3 layer between the ZrO_2 and Ge channel, which, however, inevitably leads to a larger EOT. Al_2O_3-free Ge nMOSFETs with O_3 oxidation of the Ge surface prior to ZrO_2 deposition achieve a peak μ_{eff} of 682 cm^2/V s which is higher than that of Si at the similar Q_{inv}.

Abbreviations

Ge: Germanium; ZrO_2: Zirconium dioxide; Al_2O_3: Aluminum oxide; O_3: Ozone; Si: Silicon; PMA: Post-metal annealing; PDA: Post-deposition annealing; IL: Interfacial layer; TiN: Titanium nitride; MOSFETs: Metal–oxide–semiconductor field-effect transistors; ALD: Atomic layer deposition; HF: Hydrofluoric acid; μ_{eff}: Effective carrier mobility; PPO: Plasma post-oxidation; SS: Subthreshold swing; CET: Capacitance-equivalent thickness; EOT: Equivalent oxide thickness; Qinv: Inversion charge density; HRTEM: High-resolution transmission electron microscope; Ni: Nickel; GeO_x: Germanium oxide; I_{DS}: Drain current; V_{GS}: Gate voltage; V_{TH}: Threshold voltage.

Acknowledgements

Not applicable.

Authors' contributions

LLC carried out the experiments and drafted the manuscript. HL and YP provided the discussion on the results. XY provided the discussion and revised the manuscript. GQH and YL supported the study and helped to revise the manuscript. YH provided constructive advice in the drafting. All the authors read and approved the final manuscript.

Funding

The authors acknowledge support from the National Key Research and Development Project (Grant Nos. 2018YFB2200500 and 2018YFB2202800) and the National Natural Science Foundation of China (Grant Nos. 62025402, 91964202, 61534004, 61874081, 62021004, and 62004149) and Major Scientific Research Project of Zhejiang Lab (Grant Nos. 2021MD0AC01 and 2020MD0AA01) and the Zhejiang Provincial Natural Science Foundation (Grant No. LY19F040001).

Availability of Data and Materials

The datasets supporting the conclusions of this article are included in the article.

Declaration

Competing interests

The authors declare that they have no competing interests.

Received: 25 March 2021 Accepted: 21 July 2021
Published online: 04 August 2021

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